REMARKS

Claims 1-8, 10-15 remain pending in the application. Claim 9 is canceled without prejudice. Claim 15 has been added.

Claims 1-8, 11-12 and 14 stand rejected under 35 U.S.C. 102(e) as being anticipated by Hareland et al. (U.S. Patent No. 6,909,151) (Hareland).

Applicants respectfully traverse the above rejection, and submit that Hareland teaches a semiconductor device having a body that includes a top surface and laterally opposite sidewalls formed on an insulating substrate. Hareland's structure further has a gate dielectric layer formed on the top surface of the and on the laterally opposite sidewalls of the semiconductor body. The gate electrode is formed on the gate dielectric on the top surface of the body and is adjacent to the gate dielectric on the laterally opposite sidewalls of the body. A thin film is then formed adjacent to the body, wherein a thin film produces a stress in the semiconductor body.

Applicants submit that Hareland does not teach:

a first dielectric layer covering a first portion of the substrate but does not cover a second portion of the substrate; and

a second dielectric layer having a property different from the first dielectric layer, with the second dielectric layer at least partly covering the second portion of the substrate.

Applicants submit further that the device structure of the present application has a gate formed over the second dielectric layer between the first and second doped regions.

In contradistinction, Hareland teaches "a gate formed over said second dielectric layer and between said first and second doped regions" which teaches away from Applicants' recitation of their gate. Furthermore, Hareland does not even have a first and second dielectric layers as taught by the Applicants.

Still further, Hareland requires that his device be stressed as recited in his Claim 1:

"a film formed adjacent to said semiconductor body wherein said film produces a stress in said semiconductor body".

Applicants do not teach nor suggest the presence of such stressed device. Applicants' teaches increasing the node capacitance in memory devices, such as SRAM and the like.

Hareland further requires that his gate electrode be

".... formed on said gate dielectric on said top surface of said semiconductor body and adjacent to said gate dielectric on said laterally opposite sidewalls of said semiconductor body".

Applicants' device has no such requirement.

Finally, Applicants note the remarks of the Examiner on Page 3 of the Office Action, regarding the functional limitation of

"a property of said second dielectric layer provides a gate capacitance of said gate with respect to said substrate that is greater than a theoretical capacitance of a gate formed over said first dielectric layer on said substrate".

In response, Applicants have removed this limitation from claim 1 and recite it in a newly added dependent claim 15.

In view of the foregoing, Applicants believe that Claim 1 as originally filed and all its dependent claims are not anticipated by Hareland, and respectfully request that the Examiner reconsider and withdraw the rejection of claims 1-8, 11-12 and 14 based on 35 U.S.C. 102(e).

Furthermore, The Office Action states that claims 9-10 and 13 are objected to as being dependent upon a rejected base claim, but would be allowed if rewritten in independent form including all

the limitations of the base claim.

Applicants respectfully submit that in order to advance the prosecution of the present application, claim 1 has been amended by incorporating therein the limitations recited in claim 9.

Accordingly, Applicants believe that claims 1-8, 10-15 are free of rejection under 35 U.S.C § 102(e) in view of Hareland, and respectfully request that the Examiner reconsider and withdraw the rejection of the stated claims based thereon.

In view of the foregoing, it is respectfully requested that all the outstanding objections and rejections to this application be reconsidered and withdrawn and that the Examiner pass all the pending claims to issue.

Should the Examiner have any suggestions pertinent to the allowance of this application, the Examiner is encouraged to contact Applicants' undersigned representative.

Respectfully submitted,

BRENT A. ANDERSON ET AL.

By: 

H. Daniel Schnurmann, Agent
Registration No. 35,791
Tel. No. (845) 894 2481